

CLAIMS

What is claimed is:

1 1. A method comprising:
2 predicting a first event that allows for lower performance in a processor;
3 transitioning said processor from a high performance state to a low performance
4 state upon prediction of said first event;
5 detecting a second event that can utilize greater performance in said processor;
6 and
7 transitioning said processor from said low performance state to said high
8 performance state upon detection of said second event.

1 2. The method of claim 1 further comprising detecting a cache miss event.

1 3. The method of claim 2 wherein said cache miss event causes said processor to
2 fetch data from external memory.

1 4. The method of claim 3 wherein said detecting a second event comprises
2 monitoring a bus unit for notification of incoming data from a memory fetch.

1 5. The method of claim 3 wherein said cache miss event causes said processor to
2 stall an instruction pipeline.

1 6. The method of claim 1 wherein said predicting comprises monitoring processor

2 signals indicating a cache miss, processor reset, or standby.

1 7. The method of claim 6 wherein said transitioning from a high performance state
2 to a low performance state comprises powering down idle functional units in said
3 processor.

1 8. The method of claim 1 wherein said high performance state consumes a greater
2 amount of power than said low performance state.

1 9. The method of claim 8 wherein said transitioning from a high performance state
2 to a low performance state comprises powering down functional units that are not in use.

1 10. The method of claim 9 wherein said transitioning from said low performance state
2 to said high performance state comprises powering up functional units that have been
3 powered down.

1 11. The method of claim 8 wherein said transitioning from a high performance state
2 to a low performance state further comprises slowing down an internal processor core
3 clock signal from a normal operating frequency to a lower frequency.

1 12. The method of claim 11 wherein said transitioning from said low performance
2 state to said high performance state comprises speeding up said internal processor core
3 clock signal to said normal operating frequency.

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1 13. A processor comprising:
2 a bus unit to fetch data and interact with an external bus;
3 a cache memory coupled to bus unit, said cache memory to store data;
4 an execution unit coupled to said cache memory, said execution to execute
5 instructions; and
6 a power control circuit coupled to said bus unit, said power control circuit to
7 control when said processor transitions between a high power state and a low power
8 state.

1 14. The processor of claim 13 further comprising an instruction pipeline coupled to
2 said execution unit, said instruction pipeline to provide said instructions to said execution
3 unit.

1 15. The processor of claim 14 further comprising a processor core clock generator to
2 provide a clock signal to a plurality of functional units within said processor.

1 16. The processor of claim 15 wherein said power control unit monitors said
2 execution unit and determines whether to transition said processor from said high power
3 state to said low power state.

1 17. The processor of claim 16 wherein said power control unit powers down idle
2 functional units within said processor when said processor is transitioned from said high
3 power state to said low power state.

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1 18. The processor of claim 17 wherein said power control unit monitors said bus unit,
2 and to transition said processor from said low power state to said high power state when
3 said bus unit indicates data is incoming on said external bus.

1 19. The processor of claim 18 wherein said power control unit powers up functional
2 units within said processor that have been powered down when said processor is
3 transitioned from said low power state to said high power state.

1 20. A system comprising:
2 a memory coupled to a bus;
3 a memory controller coupled to said bus;
4 a processor coupled to said bus, said processor including control logic to
5 determine whether a first event has enabled said processor to be in a low performance
6 state, to transition said processor from a high performance state to said low
7 performance state if said first even has occurred; to detect a second event
8 necessitating said processor to be in said high performance state; and to transition
9 said processor from said low performance state to said high performance state if said
10 second event is detected.

1 21. The system of claim 20 wherein said first event is a cache miss, wherein said
2 cache miss causes said processor to fetch data from said memory.

1 22. The system of claim 21 wherein said second event is bus activity due to a memory

2 read wherein said memory is sending data to said processor.

1 23. The system of claim 22 wherein said control logic is monitoring an data fetch unit
2 within said processor for cache misses and wherein said control unit is monitoring a bus
3 unit within said processor for bus activity with said memory.

1 24. The system of claim 20 further comprising a power supply to provide power to
2 said memory, said memory controller, and said processor.

1 25. The system of claim 24 wherein said power supply can sink current during a
2 transition from a high power state to a low power state, and wherein said power supply
3 can provide current during a transition from said low power state to said high power state.

1 26. An article comprising a machine readable medium having stored thereon a
2 plurality of instructions which, if executed by a machine, cause the machine to perform a
3 method comprising:

4 determining whether a first event has enabled a processor to operate in a low
5 performance state;

6 transitioning said processor from a high performance state to said low
7 performance state if said first event has occurred;

8 detecting a second event that can necessitates greater performance in said
9 processor; and

10 transitioning said processor from said low performance state to said high

11 performance state upon detection of said second event.

1 27. The article of claim 26 wherein said first event is a cache miss, wherein said
2 cache miss causes said processor to fetch data from memory external to said processor.

1 28. The article of claim 27 wherein said second event is bus activity resulting from
2 said memory send data to said processor.

1 29. The article of claim 28 wherein said method further comprises monitoring said
2 processor for cache misses and monitoring a bus for bus activity.

1 30. The article of claim 26 wherein said machine readable medium is a read only
2 memory (ROM).

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